REMARKS/ARGUMENTS

Rejection Under 35 U.S.C. § 103(a)

On page 2 of the outstanding Office action, claims 8-14 and 23 stand rejected under 35 U.S.C. § 103(a) as being obvious over Silvestri (U.S. 6,385,129) in view of Enstrom (U.S. 5,530,895).

In response to the above-stated rejection, the applicants have amended independent claims 8, 14, and 23 to recite, in combination with the other limitations, adjusting a delay based on an accuracy of the data read operations. The portions of Silvestri cited by the Office, figure 5, ref. nos. 502, 505, 511, 512, col. 1, lines 16-25, col. 5, lines 57-67, and col. 6, lines 1-3, disclose a memory device connected to a processor via a bus having address lines, data lines, and control lines. The portions of Silvestri cited by the Office do not disclose any methodologies for operating the processor or a specific hardware structure for the processor. Instead, the portions of Silvestri cited by the Office disclose "Processor 502 and memory device 504 communicate using address signals on ADDRESS lines 511, control signals on CONTROL lines 513, and data signals on DATA lines 512." The disclosure by Silvestri that the processor communicates with the memory does not establish that the processor is inherently configured to perform selecting a first group of bit lines from the bus to carry a first plurality of data patterns, selecting at least one of the remaining bit lines from the bus not within the first group to carry a second pattern or second plurality of data patterns, transmitting one or more of the first plurality of data patterns on the first group of bit lines, and transmitting one or more of the second plurality of data patterns on the at least one of the remaining bit lines. The fact that a certain result or characteristic may occur in the prior art is not sufficient to establish the inherency of that result or characteristic. To establish inherency, the extrinsic evidence must make clear that the missing descriptive matter is necessarily present in the thing described in the reference, and that it would be so recognized by persons of ordinary skill. See MPEP 2112.

Additionally, the cited portions of Silvestri disclose the memory device having a delay locked loop that can be monitored at anytime. The delay locked loop has an adjustable delay line for delaying a CLKIN signal, a model circuit for providing a delay equal to the sum of a delay

clock input buffer and a delay of one of the data output buffers to a CLKFB signal, a phase detector to detect the phase difference between the CLKIN signal and the CLKFB signal, and a controller for adjusting the delay line according to the phase difference between the CLKIN signal and the CLKFB signal. See figure 2, ref. nos. 260, 262, 266, 270, and col. 4, lines 1-10.

The CLKIN signal is produced by delaying an external clock signal with the delay clock input buffer. The CLKFB signal is produced by delaying the external clock signal with the delay clock input signal buffer, the delay provided by the adjustable delay line, and the delay provided by the model circuit. Thus, the CLKIN and CLKFB signals are produced by buffers and delay elements located in the memory device. Therefore, the adjustment of the adjustable delay line in response to a phase difference between the signals is responsive to changes in the amount of delay produced by elements located in the memory device. Further, the phase detector detects the phase difference between two signals and not the accuracy of the data read operations. Accordingly, the memory device having a delay locked loop that can be monitored at anytime, disclosed by the cited portions of Silvestri, does not render obvious adjusting a delay based on an accuracy of the data read operations. In addition to the above-stated deficiencies of Silvestri, the Office correctly points out on page 3 of the outstanding Office action that Silvestri does not disclose performing a data write/read operation at one of a plurality of storage locations using the bus after each bit in the first and the second plurality of data patterns is transmitted on respective bit lines in the bus.

The Office relies on Enstrom to teach performing a data write/read operation at one of a plurality of storage locations using the bus after each bit in the first and the second plurality of data patterns is transmitted on respective bit lines in the bus. The portions of Enstrom cited by the Office, col. 2, lines 18-67, col. 5, lines 62-67, and col. 6, lines 1-12, disclose a system for identifying interface boards connected to a computer. See figure 2, ref. nos. 12 and 26. The computer identifies the interface boards by reading the 32-bit device identifier and the 32-bit serial number stored in an address register on the interface board. See figures 2, 3, ref. no. 38 and col. 8, lines 21-26. The computer reads the 32-bit device identifier and the 32-bit serial number stored in the address register by sending a READ ID command to the interface boards. The interface boards respond to the READ ID command by reading a single address bit from its

address registers and determining if the single address bit is a logic one. See figure 3, ref. no. 46 and col. 8, lines 60-63. If the single address bit is a logic one, the board identification circuit outputs a binary 10 on the data bus. See figures 2, 3, ref. no. 36, col. 8, lines 63-67 and col. 9, lines 1-4. The computer then repeats the READ ID command for the same single address bit and the interface boards having a logic one for the single address bit output a binary 01 on the data bus. See col. 9, lines 4-11.

The system for identifying interface boards connected to a computer disclosed by the portions of Enstrom cited by the Office does not perform data write/read operations using the first and second data patterns. Instead, the system uses the first and second data patterns to represent a binary one of the device identifier and the serial number of the interface board to ensure that noise on a floating data bus does not cause the device identifier and the serial number to be misinterpreted. Additionally, the first and second data patterns represent a binary one of the device identifier and the serial number and the binary one is written to memory and not the first and second data patterns. See col. 11, lines 4-17. Therefore, the combination of Silvestri and Enstrom fails to disclose or suggest the applicants' claimed invention. Accordingly, it is believed that independent claims 8, 14, and 23 as well as dependent claims 3, 7, 9-10, 12, 16-22, and new claims 24-30 are in condition for allowance.

New claim 27 is a method claim having subject matter which corresponds with the subject matter of claim 14. Certain dependent claims have also been added which contain subject matter similar to the other dependent claims. No new matter has been added.

At the time this application was filed, the application contained 23 total claims, 4 of which were independent. The application, after the instant amendment, contains 22 total claims, 4 of which are independent. Accordingly, no additional claims fee is believed to be due.

On page 4 of the outstanding Office action, claims 3, 7, and 17-22 are rejected under 35 U.S.C. § 103(a) as being obvious over Silvestri (US 6,385,129) in view of Enstrom (US 5,530,895) and, further, in view of Medlock (US 6,567,017). The applicants respectfully point the Office to the above-stated remarks concerning the deficiencies in the combination of Silvestri in view of Enstrom as applied to independent claims 8, 14, and 23. In view of the above-stated

deficiencies in the combination of Silvestri in view of Enstrom, it is respectfully submitted that dependent claims 3, 7, and 17-22 are in condition for allowance.

Applicants have made a diligent effort to place the instant application in condition for allowance. Accordingly, a Notice of Allowance for pending claims 3, 7-10, 12, 14, and 16-30 is respectfully requested. If the examiner is of the opinion that the instant application is in condition for disposition other than through allowance, the examiner is respectfully requested to contact applicants' attorney at the telephone number listed below.

Respectfully submitted,

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